



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Mark A. Anders, et al. Art Unit : 2814
Serial No.: 09/895,278 Examiner : Dana Farahani
Filed : June 29, 2001 Notice of Allowance Date:
Assignee : Intel Corporation March 31, 2005
Title : DYNAMIC BUS REPEATER WITH IMPROVED NOISE TOLERANCE

Mail Stop Issue Fee

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE OF ALLOWANCE

In response to the Notice of Allowance mailed March 31, 2005, enclosed are a completed issue fee transmittal form PTOL-85b and a check for \$1,700 for the required fee.

COMMENTS ON EXAMINER'S REASONS FOR ALLOWANCE

It is agreed that the limitations recited in the examiner's Reasons for Allowance are not taught or suggested by the art of record, and that the allowed independent claims 1 and 11 are distinguished from the cited prior art for at least the reasons stated in the Reasons for Allowance. Applicant does not concede that the stated reasons are the only grounds for patentability of the allowed claims, that the limitations excluded from the

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

May 10, 2005

Date of Deposit

Signature

Jennifer H. Payne

Typed or Printed Name of Person Signing Certificate

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Reasons for Allowance are taught or suggested by the art of record, or that all of the limitations are necessary for patentability of the allowed claims or other claims directed to the disclosed subject matter. For example, other claims including different limitations are patentable over the cited prior art.

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REMARKS

Claims 1-5 and 7-17 are allowed.

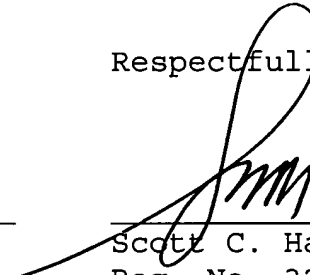
The drawings were objected to under 37 C.F.R. §1.83(a) for failing to show features of the invention as specified in the claims. Applicants respectfully traverse the objection.

Applicant claims an input transistor sized in such a ratio that enables an output voltage of $V_{cc}/2$ in response to an input voltage of $V_{cc}/2$ on the input node in the evaluate mode. The input of $V_{cc}/2$ is shown in Figure 6 as input to the gate of the transistor 524. Applicants submit that the drawings as filed on June 29, 2001 therefore support $V_{cc}/2$. An issue notification is respectfully solicited.

Please apply any charges or credits to our Deposit Account No. 06-1050.

Respectfully submitted,

Date: May 10, 2005



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